What is Claimed is:

1. A logic block in a field programmable gate array, comprising:

a plurality of clusters of logic devices, at least one of said logic devices in each of said plurality of clusters having an input or an output;

a first set of interconnect conductors entering said logic block from a first side and forming a programmable intersection with said input or said output of said at least one of said logic devices in each of said plurality of clusters;

a second set of interconnect conductors entering said logic block from a second side and forming a programmable intersection with said input or said output of said at least one of said logic devices in each of said plurality of clusters, said first set of interconnect conductors forming a pail-wise hardwired connection with said second set of interconnect conductors; and

an interconnect conductor splitting extension disposed between said first set of interconnect conductors and said second set of interconnect conductors.